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THE RESEARCH OF CLASS E POWER AMPLIFIER MODEL WITH HIGH EFFICIENCY

The paper deals with the process of the design procedure and implementation of a modern switch-mode class E power amplifier model that theoretically could give up to 100 % efficiency due to minimizing the power dissipated during the transistor on-off transition, even if the switching time of it takes a significant fraction of the signal period. The primary purpose was designing an effective mathematical model, based on which it can be possible to obtain a practical model of class E amplifier with parameters corresponding with calculated. Mathematical calculations gave us results with an accuracy of 98 %, converging with the practical measurements. According to analytical calculations with quality factor 8, the output load current is sinusoidal (–20dB second harmonic). Modeling results confirmed the methodology of calculation and the practical model was used to design a laboratory stand for studying and researching class E amplifiers.

Keywords: *class E amplifier; class E model; power efficiency; output amplifier.*

У статті розглядається процес розробки та реалізації сучасної моделі ключового підсилювача класу Е, що теоретично може видавати до 100 % ККД завдяки мінімізації розсіюваної потужності впродовж часу включення-виключення транзистору, навіть якщо його час переключення займає значну частину періоду сигналу. Головною метою було створення ефективної математичної моделі, на основі якої можливо отримати практичний зразок підсилювача класу Е з параметрами, що точно відповідають розрахунковим. Математичний розрахунок дозволив отримати результати, які з точністю 98 % збігаються з практичними результатами вимірювання. Згідно аналітичного розрахунку з навантаженою добротністю 8, вихідний струм навантаження є синусоїдальним(–20dB друга гармоніка). Результати вимірювань підтвердили методику розрахунку і практична модель була використана для створення лабораторного стенду для вивчення та дослідження підсилювачів класу Е.

Ключові слова*: підсилювач потужності класу Е; модель класу Е; ККД; вихідна потужність.*

Problem's Formulation

Radiofrequency power amplifiers are used mainly to increase signal power to obtain the required characteristics of that signal and are the main consumers of devise power. That's why output amplifiers of transmitting equipment have significant importance in the view of power efficiency, as they are the main consumers of energy in such devices.

Previous classes of amplifiers cannot operate on high frequencies with decent efficiency (A, B, AB, C) or place active device in undesirable conditions (class D). Reducing power losses in high-power output amplifiers and battery energy preservation is essential for portable or remote mobile devices.

Switching modes are characterized by higher efficiency than current source amplifiers because the use of transistor in linear A, B, AB, C classes of amplifiers as a current source requires that the

minimum voltage across the transistor's output pins must be greater than a particular value while passing current, in order not to enter non-linear zone of volt-ampere characteristic, which leads to an increase in waste power dissipation and harmonic distortions in output signal [8]. The main advantages of the class E switch power amplifier proposed sample are: low cost, small size, relatively high efficiency, uncomplicated design, quite high reliability, low sensitivity to transistor characteristics, transistor ability to operate at much smaller on voltage and perspective for high-efficiency high-frequency functioning.

As well known when designing power circuits in amplifiers, dissipative elements must be avoided in order to increase power efficiency [4]. Class-E is based on a reactive elements and load circuit developed to have a transient process that increase power efficiency even if the transistor switching times are a substantial part of the signal cycle (turn-on up to about 30 % of the period and turn-off transition up to about 20 % of the period [6]). The maximum useful frequency for the low-order Class E is a frequency at which the transistor turn-off switching time is about 17 % of the period. Therefore, a low-order Class-E circuit will work well with a particular transistor at frequencies up to about 70 % of the frequency at which that transistor works well in a Class-B amplifier [6]. Harmonic output and power gain are comparable with conventional amplifier classes (total harmonic distortion THD is the same as class B). Suppose it will be necessary to obtain harmonic output significantly below the main frequency. In that case, any amplifier other than Class A or push-pull Class AB cannot operate within a band wider than 1.8:1 with only one fixed-tuned harmonic suppression filter [3]. Class E is used in wireless technology and GSM-signal transmitters [9—13].

Analysis of recent research and publications

The [8] describes the peculiarities of the realization of the high-efficiency modes of SHF power transistor amplifiers. The author warns that obtaining the desired increase in efficiency can be impossible because of the lack of the level of transistor harmonic generation and asserts that nonlinearity is necessary to create power dissipation minimization conditions. The peculiarities and disadvantages of previous high-frequency class C amplifiers were described in [4]. The main principles of building a class E power amplifier sample with 83 % efficiency working on 800 kHz and the practical scheme were described in [7].

The implementation of the switching mode up to frequencies when the transistor switching time is 32 % of the signal period firstly was described and the definition "class E" was introduced in [1]. As well-known transistor power dissipation is equivalent to voltage multiplied by current and integrated through the whole high-frequency period [2]. For high-efficiency amplifiers the conditions for obtaining maximum efficiency and maximum output power P_{out} usually don't match [7]. It is proper to notice that the impedances at f are the most influential; the impedances at harmonic frequencies have correspondingly less contribution to the voltage waveforms. The importance was obvious: lower loaded quality factor Q_L led to larger harmonic output, higher efficiency, wider frequency regulation across the band, and stricter requirement of output filter. Meanwhile, higher Q_L gave less harmonic output, less efficiency, and more narrowed frequency band regulation [1].

Relevant tasks include researching and designing class E amplifier as the main output part of transmitting devices.

Formulation of the study purpose

The main aims of the work are next: to study the processes in class-E amplifier, develop the numerical model, create and investigate the program model, and develop a model sample of class-E power amplifier with high efficiency. This model is used for designing of a laboratory stand for studying and researching class E amplifiers.

Presenting main material

The main principles of minimizing transistor losses in class E amplifiers [1] are:

1) reducing the voltage across the transistor when current runs through it;
2) reducing the current flow through the transistor when voltage presents across it;
3) reducing the duration of any unavoidable conditions during which precious current and voltage across the transistor are present at the same time.
4) the delay of voltage rising while the transistor turns off must be long enough in order to guarantee that the current through the transistor has by that time reduced almost to zero.

5) to provide zero voltage returning and current rising delay when the transistor turns on.
6) to minimize the voltage slope as possible at the time when the transistor turns on ($dV_{DS}/dt \approx 0$, where V_{DS} — drain-source voltage).

Input signal waveform can be optimized according to efficiency, adjustment, and power gain criteria. The switch initial duty ratio is made approximately 50 percent and by adjusting it we step by step get closer to the optimal value. But even with the proper choice of the adjustments and the transistor, the switching time of it may take a considerable part of the signal cycle in violation of Condition 3) [4]. Conditions 1) and 2) are quite independent of the load circuit design. It is remarkable, that in this case, the condition of fully matching the transistor and the load resistances at the fundamental frequency is not only not dominant, but also leads to incorrect tuning. The complete circuitry is presented in fig. 1.

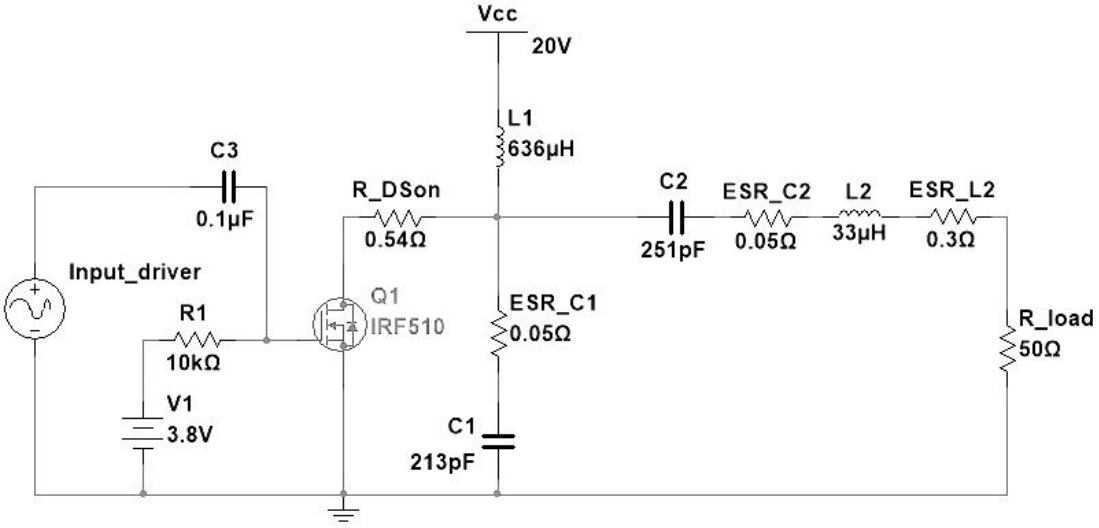


Fig. 1. The schematic of class-E power amplifier with the parasitic resistances

From fig. 1 we can see that parasitic resistances are included in circuitry: $R_{DS(on)}$ — drain-source on resistance; ESR_{C1}, ESR_{C2}, ESR_{L2} — equivalent series resistances of C_1, C_2, and L_2 correspondingly; V_{CC} — power supply voltage. The capacitor C_1 includes the transistor output capacitance and the circuit intrinsic capacitance and also prevents rapid voltage increase across the transistor after the drain current has reduced to zero. Zero voltage slope during transistor turn-on permits accidental slight mistuning across the radiofrequency band without severe loss of efficiency and stress conditions. Furthermore, the conditions $V = 0$ and $dV_{DS}/dt = 0$ at the end of the "off" state $t = (1\text{-}D)(1/f)$, where D = 0.5 is the pulse duration, together imply that the transistor current at the start of the "on" state will be zero and will increase only gradually. Despite imperfect transistor characteristics, the turn-on will be relatively slow, which will not place the transistor in undesirable conditions and will help to minimize the duration of the whole transistor turning-on process. Leakage inductance can be included in L2 and/or L_1, which is a high-reactance shunt-feed choke. Loaded quality factor Q_L for given frequency $f = 1.9MHz$ here is defined as [6]:

$$Q_L = \frac{2\pi f L_2}{R}, \tag{1}$$

where R — is the collective resistance of ESR_{C2}, ESR_{L2}, R_{load}, R_{load} — is the load resistance and will be considered further. The typical range of Q_L values is from 5 to 30 (optimum value 8-10) [5]. It is desirable to choose L_2 slightly higher than the optimal value, to allow the output current to assist in turning on the transistor (if bipolar one is used) [1].

The loss of power in the $R_{DS(on)}$ and partially charged C_1 during discharging are not functions of the design frequency. If we increase the design frequency for given types of C or L components, losses will: in capacitor ESRs increase, inductor core losses increase, and inductor winding losses

decrease [6]. The nearly sinusoidal fundamental frequency current flows through the branch L_2-C_2-R_{load}, the percentage harmonic distortion in this current is approximately inversely proportional to Q_L (The harmonic content is primarily the second harmonic, with amplitude $\approx 0.51/Q_L$ regarding the fundamental). The part of AC power that is lost as power dissipation in reactive components can be found from [5] as Q_L/Q_U , where Q_U is the unloaded network Q. A specific C_1/C_2 ratio (6,7) makes the chosen Q_L provide the proper damping, resulting to zero-slope V_{DS} at turn-on time.

Calculations of design equations can be made only by assuming that the current in L_2-C_2 is sinusoidal, that is strictly true only if the load circuit has infinite Q_L. The values of R and V_{CC} are dependent on the requirement to deliver a specified output power P_{out} to the load. Output power also depends secondarily on Q_L. In case this dependence is ignored [1] we can obtain from 10 % to 38 % less output power from what we expect. In order to compensate this, some amendments can be made to coefficient calculations of C_1, C_2, and P_{out} depending on Q_L. To make accurate circuit designs at any arbitrary value of Q_L, the developer needs design equations to comprise continuous mathematical functions, rather than a set of tabulated values as in Table 1 in [6]. Such equations are given further for lossless components [3].

The effective direct current (DC) DC-supply voltage (V_{CC}–$V_{t(sat)}$, where $V_{t(sat)}$ — transistor saturation voltage) is the actual voltage and more than the transistor on voltage-saturation, hence in our case $V_{t(sat)}$ is zero for a field-effect transistor. From [6] we can calculate output power with a third-order polynomial which gives higher accuracy within -0.0089 % to +0.0072 %:

$$P_{out} = \frac{(V_{CC} - V_{t(sat)})^2}{R}\left(\frac{2}{\frac{\pi^2}{4}+1}\right) f(Q_L) = 0.576801\frac{(V_{CC} - V_{t(sat)})^2}{R} \times \tag{2}$$

$$\times [1.001245 - \frac{0.451759}{Q_L} - \frac{0.402444}{Q_L^2} + \frac{0.205967}{Q_L^3}].$$

It is remarkably that R comprises all the parasitic resistances of the elements [6]:

$$R = R_{load} + ESR_{L2} + ESR_{C2} + 1.365R_{DS(on)} + 0.2116ESR_{C1} \tag{3}$$

and can be calculated:

$$R = 0.576801\frac{(V_{CC} - V_{t(sat)})^2}{P_{out}}[1.001245 - \frac{0.451759}{Q_L} - \frac{0.402444}{Q_L^2} + \frac{0.205967}{Q_L^3}]. \tag{4}$$

The desired Q_L may be chosen freely (~ 5-10, but not less than 1.7879 [6]), according to the design compromise between efficiency and harmonic content of the power delivered to the load. Then we can find other components:

$$L_2 = \frac{Q_L R}{2\pi f}, \tag{5}$$

$$C_1 = \frac{1}{2\pi f R\left(\frac{\pi^2}{4}+1\right)\left(\frac{\pi}{2}\right)}\left[0.99866 + \frac{0.91424}{Q_L} - \frac{1.03175}{Q_L^2}\right] + \frac{0.6}{(2\pi f)^2 L_1} = \tag{6}$$

$$= \frac{1}{34.2219 f R}\left[0.99866 + \frac{0.91424}{Q_L} - \frac{1.03175}{Q_L^2}\right] + \frac{0.6}{(2\pi f)^2 L_1};$$

$$C_2 = \frac{1}{2\pi f R}\left(\frac{1}{Q_L - 1.104823}\right)\left[1.00121 + \frac{1.01468}{Q_L - 1.7879}\right] - \frac{0.2}{(2\pi f)^2 L_1}. \tag{7}$$

These equations (2)—(4), (6)—(7) are more accurate than previous from [1]. It is important to notice that L_2 is not resonant with C_2 at f or with the series combination of C_1 and C_2. Load reactance is absorbed into C_2 and L_2. Inductive resistance X_{L1} usually is 30 or more times bigger than the unadjusted value of capacitive resistance X_{C1}[6]:

$$L_1 = \frac{30}{(2\pi f)^2 C_1}. \tag{8}$$

The DC drain current of the transistor, while delivering ac power P_{out}, is

$$I_{DC} = \frac{P_{out}}{V_{CC}} \left[\frac{1 - \frac{(2\pi A)^2}{12}}{1 - \frac{(2\pi A)^2}{6} - \frac{V_{t(sat)}}{V_{CC}} \left(1 + A - \frac{(2\pi A)^2}{6} \right)} \right], \tag{9}$$

where A is:

$$A \equiv \left(1 + \frac{0.82}{Q_L} \right) f t_f \tag{10}$$

and where t_f is the collector current fall time during transistor turn-off. The drain current wave shape is determined by the load circuit and is approximately a section of a sine wave (between –32.5° and +147.5° in angle) centered at $I = I_{DC}$. The current builds up gradually from zero at the beginning of the "on" half-cycle to a peak value of [5]:

$$I_{Dpk} = I_{DC} \left[1 + \left(\frac{\pi^2}{4} + 1 \right)^{\frac{1}{2}} \left(1 - \frac{0.5}{Q_L} \right) \right] = I_{DC} \left[1 + 1.862 \left(1 - \frac{0.5}{Q_L} \right) \right]. \tag{11}$$

It then decays gradually to cut-off current:

$$I_{off} = 2 I_{DC} \left(1 + \frac{0.82}{Q_L} \right). \tag{12}$$

For maximum efficiency, the highest possible V_{CC} should be used, within the V_{DS} transistor limitation. The peak drain-source voltage V_{DSpk} is found [5]:

$$V_{DSpk} = V_{CC} + \left[2\pi \arcsin\left(\frac{\pi^2}{4} + 1 \right)^{-\frac{1}{2}} - 1 \right] \left[V_{CC} - V_{t(sat)} \right] = 3.562 V_{CC} - 2.562 V_{t(sat)}. \tag{13}$$

The maximum V_{CC} can be consequently found for particular transistor:

$$V_{CC} = \frac{2.562 V_{t(sat)} + V_{DSpk}}{3.562}. \tag{14}$$

These peak and direct current values must be within the safe operating datasheet characteristics of the transistor. The most stressful condition is linear turnoff at $\approx 2 I_{DC}$.

Using MOSFET or MESFET transistors drain efficiency can be calculated [6]:

$$\eta_D = \frac{R_{load}}{R_{load} + ESR_{L2} + ESR_{C2} + 1.365 R_{DS(on)} + 0.2116 ESR_{C1}} - \frac{(2\pi A)^2}{12} - x - 0.01, \tag{15}$$

0.01 reserves additional unaccounted losses (this number can be higher).

Class E characteristics are highly dependent on load circuit adjustment, so to operate across a frequency band, adjustments may be made for C_1, C_2, L_2 or fixed elements can be used with some sacrifice of performance. The possible need for tuning comes from tolerances in the component values and the high possibility of undefined value inductive and capacitive reactances inserted in series with R_{load}. Those series reactances require the L_2 and C_2 to be reduced by the amounts of the unknown inserted inductive and capacitive series reactances, so it can be possible to adjust them so as to fulfill simultaneously the two desired conditions even if these reactances are undetermined.

A power loss of x fraction of the normal DC input power due to non-zero "off"-state current can be calculated from [6]:

$$x = \frac{I_{Doff}}{I_{DD}[1/(1-D)]}. \tag{16}$$

The driver turns off the transistor from 100 % to 0 % of the fall-time t_f fast enough to make the turn-off power dissipation as a much possibly smaller fraction of the output power as it can be. This fraction is $(2\pi A)^2/12$, which estimates an acceptable part of the output power to be dissipated during the non-zero turn-off switching time.

According to the described formulas the calculations have been made with the following results for *1.9MHz* frequency: P_{out} *= 4.307W,* L_2 *= 34.1774uH,* C_1 *= 246.354pF* (excluding IRF510 transistor drain-source capacitance 91pF), C_2 *= 275.176pF,* L_1 *= 636.49uH,* I_{DC} *= 0.2166A,* I_{Dpk} *= 0.6088A,* I_{off} *= 0.4758A,* V_{DSpk} *= 71.24V,* $\square_D$ *= 0.9632.*

Analytical calculations allowed us to make the idealized model in NI Multisim14 Education edition program (fig. 2).

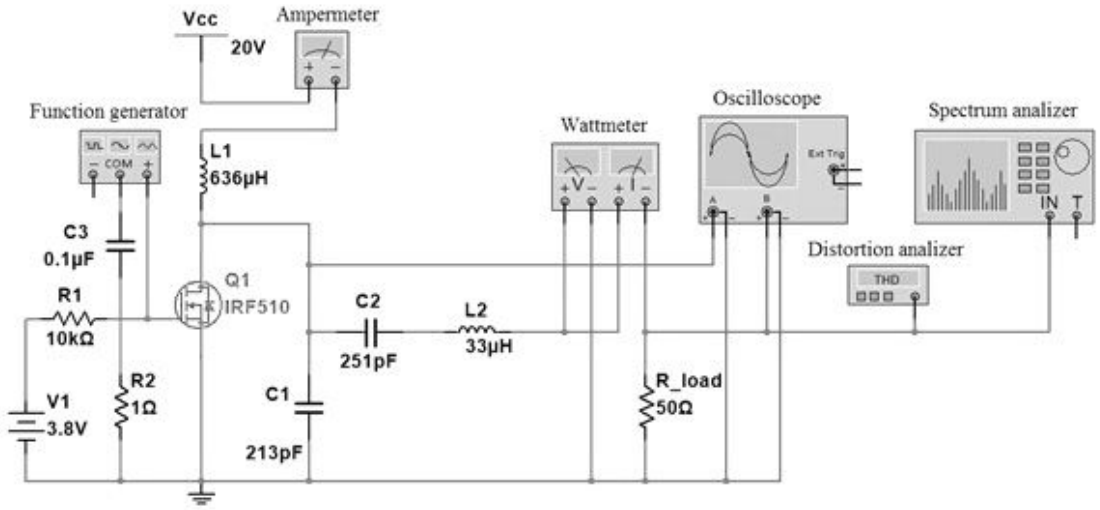


Fig. 2. The idealized class-E power amplifier model in the NI Multisim program

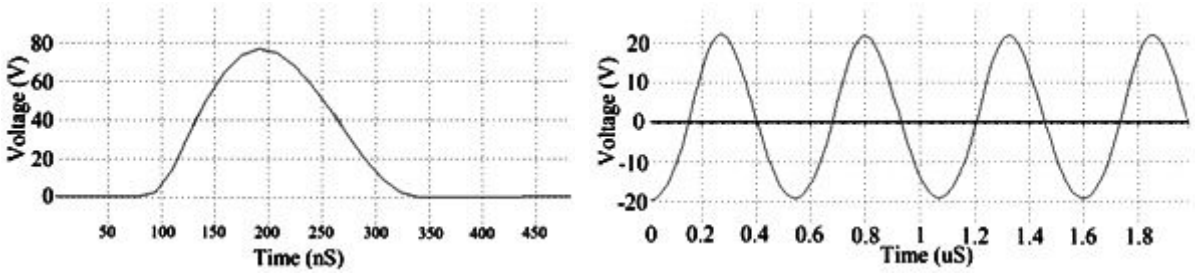
Multisim is an industry-standard SPICE (Simulation Program with Integrated Circuit Emphasis) simulation and circuit design software for analog, digital, and power electronics for education and research purposes. It includes industry standard SPICE simulation with an interactive schematic workspace to visualize and analyze electronic circuit peculiarities. It has a useful interface that allows students strengthen circuit theory and improve memorization of theory during engineering studies. Many developers, researchers, and designers use Multisim to reduce PCB prototype iterations and reduce development value by adding high-productive circuit simulation and analyses to the design process [14].

Being quite hard to supply the transistor gate with a square wave signal at such frequencies, this amplifier is supplied with a sinusoidal signal, and a bias gate circuit is also added for duty cycle regulation and for different transistor turn-on/off delays compensation. To fulfill this requirement the zero-level (DC constant bias) of the sine-wave should be positioned slightly under the transistor turn-on threshold voltage.

Further research of the model gave us the next results (fig. 3): P_{out} *= 4.312W,* L_2 *= 33uH,* C_1 *= 213pF +* internal transistor output capacity, C_2 *= 251pF,* L_1 *= 636uH,* I_{DC} *= 0.2214A,* V_{DSpk} *= 76.8V, THD = 7.4 %* (total harmonic distortion), $\square_D$ *= 0.9738.*

On the spectral diagram (fig. 4) we can see –19dB reduction of the second harmonic, –35dB reduction of the third, and –47dB reduction of the fourth harmonic.

Based on theoretical calculations and program modeling, the practical sample model as part of the laboratory stand for class E amplifier investigation was built (fig. 5).



(a) the drain voltage waveform (b) the output signal waveform

Fig. 3. The model investigation results

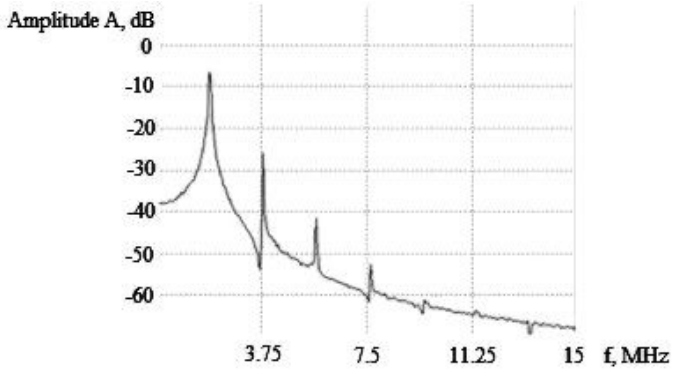


Fig. 4. The output signal spectral diagram of the program model

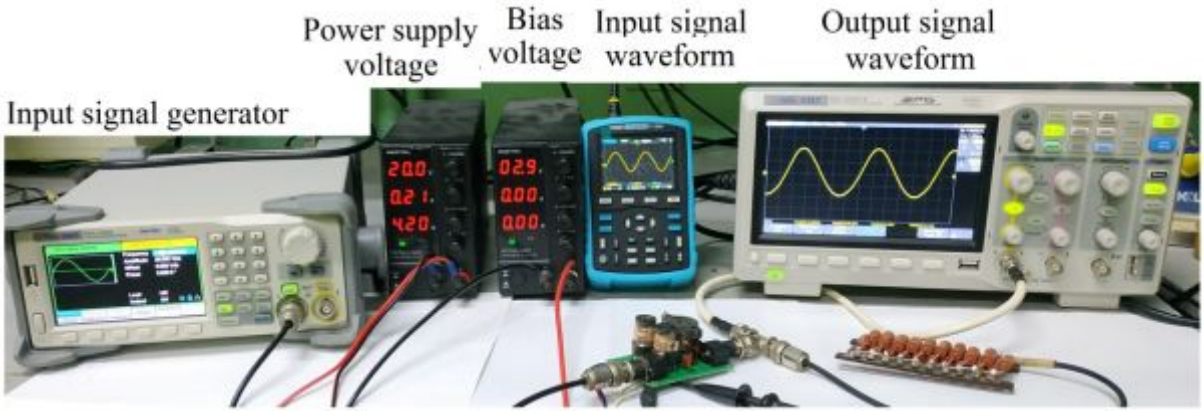
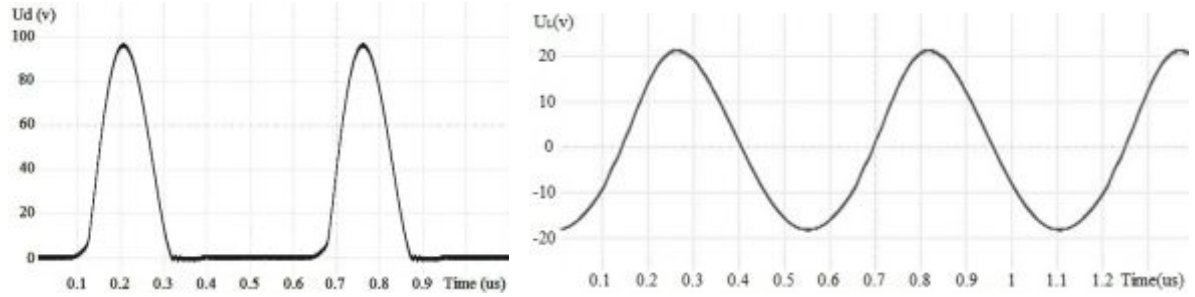


Fig. 5. Laboratory stand for class E amplifier investigation

The laboratory stand allows supplying of the amplifier with input signal up to 20 V, accurate regulation of input frequency up to 60 MHz, voltage and bias supply up to 30 V, and accurate input and output signal measurements. The stand includes the following devices:

- The input signal generator Siglent SDG 1000X
- The power supply voltage Wanptek NPS306W
- The bias voltage supply Wanptek NPS306W
- The input signal oscilloscope Fnirsi DPOX180H
- The output signal oscilloscope Siglent SDS 1202X-E

Assembling and investigation of the practical sample gave us next element values: P_{out} = *4.2W*, L_2 = *33.9uH*, C_1 = *100pF* + internal transistor output capacity, C_2 = *270pF*, L_1 = *400uH*, I_{DC} = *0.22A*, V_{DSpk} = *74.5V*, $\square_D$ = *0.95*. In fig. 6a we can see the classic drain voltage waveform U_d with a bit of ringing during “on” time. fig. 6b shows us the output voltage waveform on active load.



a b

Fig. 6. Drain voltage waveform U_d (a), output signal voltage waveform U_L (b)

From fig. 6a we can observe increasing in the drain peak voltage on 18.4 V compared to the program model (fig. 3a) and the output voltage of the practical sample (fig. 6b) show us accurate convergence with the model depicted in fig. 3b.

Different transistors were also implemented with the following results (Tabl. 1).

Table 1. The practical results with the different transistors

Name	P_{out}, W	C_1, pF	V_{DSpk}, V	η_D
FQPF12N60C	*20.25W*	100	270	*0.767*
STP10NK60ZFP	*19.36W*	120	230	*0.88*
IRF740	*19.36W*	120	230	*0.88*
20N60C3	*23W*	120	250	*0.853*
SSP6N60	*19.36W*	120	250	*0.8*
B6NA60FI	*19.36W*	120	230	*0.806*

As we can see, relatively less efficiency of the FQPF12N60C transistor caused by higher turn on-off time. The best efficiency results were obtained with the STP10NK60ZFP and the IRF740 transistors, which further can be used for building medium power output amplifiers for radio transmitters.

In fig. 7 we can observe the output signal spectral diagram (Siglent SDS 1202X-E), which gave us an impression of the harmonic content and amplifier behavior.

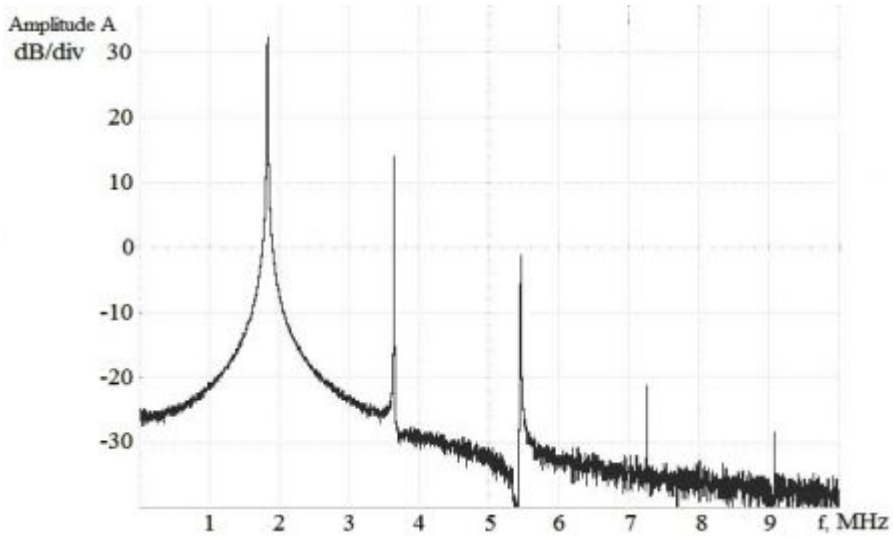


Fig. 7. The output signal spectral diagram of the amplifier practical sample

Fig. 7 shows us –18dB reduction of the second harmonic, –34dB reduction of the third, and –54dB reduction of the fourth harmonic, which differs by 5.2 % for the second harmonic, 2.8 % for the third, and 13 % for the fourth harmonic with program model (fig. 4).

The main results of the conducted investigations are presented in Tabl. 2.

Table 2. Summary of results of investigation of class E amplifier

	f, MHz	P_{out}, W	C_1, pF	C_2, pF	L_1, μH	L_2, μH	I_{DC}, A	V_{DSpk}, V	η_D
Calculations	1.9	4.307	246.3	275.1	636.4	34.17	0.216	71.24	0.963
Program model	1.9	4.312	213	251	636	33	0.221	76.8	0.973
Practical sample	1.9	4.2	100	270	400	33.9	0.22	95.2	0.95

Conclusions

The processes in the class E power amplifier were studied, the numerical model was developed, and the model sample was designed, simulated, and is used in laboratory stand for class E amplifier research. Also, due to the impossibility of controlling the higher harmonics infinity number, such signal forms differ from “ideal” ones, but load current is fairly sinusoidal as it was considered in the analytical design procedure, so all design approximations(calculations) made were confirmed. A 95 % efficiency was obtained, besides IRF510, STP10NK60ZFP and IRF740 transistors also can be used efficiently for designing medium-power high-frequency radio transmitters. The laboratory stand allows accommodating different brands of MOSFET and IGBT transistors easily. Modeling and practical results demonstrated accuracy and convergence within 2 % in efficiency, the highest deviation was 25 % for V_{DSpk}, the transistor stays in the safe operating area and this amplifier could be used as a part of the portable radio transmitter or for further student research works as part of the laboratory stand.

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ДОСЛІДЖЕННЯ МОДЕЛІ ПІДСИЛЮВАЧА КЛАСУ Е З ВИСОКИМ ККД

Реферат

У статті розглядається процес розробки та реалізації сучасної моделі ключового підсилювача потужності класу Е для діапазону 1,8 МГц з вихідною потужністю 4,3 Вт, який теоретично може забезпечити до 100 % ефективності в ідеальному випадку завдяки мінімізації потужності, що розсіюється під час перехідного процесу транзистору, навіть якщо час перемикання транзистора становить значну частину періоду сигналу. Основними перевагами пристрою є: відносно високий ККД, неускладнена конструкція, досить висока надійність, низька чутливість до характеристик транзистора, здатність транзистора працювати при значно меншій напрузі та перспектива для високоефективного високочастотного функціонування.

Основною метою було розробити, дослідити та побудувати корисну та практичну модель підсилювача класу Е з високою енергоефективністю, яка в подальшому буде використовуватися як частина лабораторного стенду для практичних і лабораторних робіт студентів з курсу «Радіопередавальні пристрої».

Аналітичний огляд дав нам точний розрахунок основних компонентів і процесів, що допомогло уникнути використання транзистора в небажаних режимах і мінімізувало тривалість всього процесу переключення транзистора. Залежність була підтверджена практично: нижча навантажена добротність Q_L призвела до більшого виходу гармонік, вищої ефективності, ширшого регулювання частоти в смузі, тим часом як вища Q_L дала менший вихід гармонік, меншу ефективність, більш звужену можливість регулювання частоти в діапазоні. Вихідна потужність також вторинно залежить від Q_L — в разі ігнорування цієї залежності ми можемо отримати від 10 % до 38 % менше вихідної потужності від розрахункової.

Ретельний опис і розрахунки дали результати з точністю 2 %, струм навантаження як в моделі, так і в зразку є синусоїдальним з визначеним рівнем спотворення, як це було передбачено в процесі аналітичного проектування ($Q_L = 8$). Усі дослідження і моделювання підтверджені практично, транзистор залишається в безпечній робочій зоні, а експериментальний пристрій може використовуватися як частина радіопередавального обладнання низької потужності та як частина лабораторного стенду для здобувачів вищої освіти для дослідження особливостей і властивостей підсилювача класу Е.

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